# Refine Search

Search Results -

Terms Documents
L2 and silane 2

US Pre-Grant Publication Full-Text Database
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Database:

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JPO Abstracts Database
Derwent World Patents Index
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Search:

L5

Refine Search

Recall Text 👄

Clear

Interrupt

### Search History

DATE: Thursday, June 24, 2004 Printable Copy Create Case

Set Nam ide by sid	<u>e Query</u> le	Hit Count S	<u>set Name</u> result set
DB=U	ISPT; PLUR=YES; OP=ADJ		
<u>L5</u>	L2 and silane	2	<u>1.5</u>
<u>L4</u>	L3 and silane	0	<u>L4</u>
<u>L3</u>	L2 and (hard adj mask)	11	<u>1.3</u>
<u>L2</u>	L1 and polysilicon	74	<u>L2</u>
<u>L.1</u>	sequentially near9 (tunnel adj oxide)	83	<u>L.1</u>

**END OF SEARCH HISTORY** 

## **Hit List**

Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs
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### Search Results - Record(s) 1 through 2 of 2 returned.

1. Document ID: US 6649965 B2

L5: Entry 1 of 2

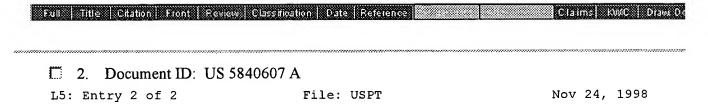
File: USPT

Nov 18, 2003

US-PAT-NO: 6649965

DOCUMENT-IDENTIFIER: US 6649965 B2

TITLE: Semiconductor device and method of manufacturing the same



US-PAT-NO: 5840607

DOCUMENT-IDENTIFIER: US 5840607 A

TITLE: Method of forming undoped/in-situ doped/undoped polysilicon sandwich for

floating gate application

Full	Title Citation Front Review Cla	ssification Date Reference Claims DMC Draw	Ō.
Clear	Generate Collection	Print Fwd Refs Bkwd Refs Generate OACS	 
	Terms	Documents	
	L2 and silane	2	

Display Format: TI Change Format

Previous Page

Next Page

Go to Doc#

#### First Hit Fwd Refs

Generate Collection Print

L5: Entry 1 of 2 File: USPT Nov 18, 2003

DOCUMENT-IDENTIFIER: US 6649965 B2

TITLE: Semiconductor device and method of manufacturing the same

#### Detailed Description Text (7):

Then, a first silicon film 3 made of <u>polysilicon</u> and serving as a part of the floating gate is grown on the tunnel oxide film 2 by the CVD method to have a thickness of 10 nm. In this growing, phosphorus is doped into the first silicon film 3 to get an impurity concentration of 0.5.times.10.sup.20 atm/cm.sup.3, for example. Phosphine (PH.sub.3) is employed as the phosphorus doping gas.

#### Detailed Description Text (17):

Then, as shown in FIG. 2G and FIG. 3C, a second silicon film 8 made of polysilicon is selectively grown on the first silicon film 3. As the selective growth method, for example, a dichlorsilane-series gas or a mixed gas consisting of the dichlorsilane-series gas and a chlorine-series gas (e.g., hydrochloric acid) is used. The reason for using such gas series is that the silicon constituting dichlorsilane (SiH.sub.2 Cl.sub.2) acts as a growth element of the polysilicon whereas the chlorine constituting dichlorsilane or the chlorine in a hydrochloric acid-series gas as an addition gas has an action to etch the silicon. Accordingly, such gas has an action of suppressing the nuclear growth of the silicon on the surface of the device isolation insulating film 7 and also an action of selectively growing the second silicon film 8 on the first silicon film 3.

#### <u>Detailed Description Text</u> (30):

Then, as shown in FIG. 2I and FIG. 3E, an undoped and <u>polysilicon</u> third silicon film 10 of 150 nm thickness and a second silicon nitride film 11 of 20 nm thickness are grown sequentially over the silicon substrate 1 by the CVD method. As described later, the impurity is introduced into the third silicon film 10 when such impurity is ion-implanted to form the impurity diffusion layer in the silicon substrate 1.

#### Detailed Description Text (60):

First, like the first embodiment, the tunnel oxide film 2 and the first silicon film 3 made of polysilicon are formed on the silicon substrate 1. In this case, the thickness of the first silicon film 3 is set to 20 nm and the phosphorus concentration is set to 0.5.times.10.sup.20 atm/cm.sup.-3.

#### Detailed Description Text (67):

Then, as shown in FIG. 5E and FIG. 6B, the second silicon film 8 made of <u>polysilicon</u> is formed selectively on the first silicon film in the device forming regions by employing the similar method shown in the first embodiment.

### Detailed Description Text (69):

Then, as shown in FIGS. 6C and 6D, the ONO film 9, the third silicon film 10 made of polysilicon, and the second silicon nitride film 11 are formed on the second silicon film 8 and the device isolation insulating film 7. In turn, the control gate CG and the floating gate FG are formed by patterning the films from the third silicon film 10 to the first silicon film 3. Since subsequent steps are similar to those in the first embodiment, their explanation will be omitted.

#### Detailed Description Text (74):

First, like the second embodiment, the <u>tunnel oxide film 2</u> and the <u>first silicon film 3</u> are formed sequentially on the <u>silicon substrate 1</u>, then the <u>tunnel oxide</u> film 2 and the first silicon film 3 are patterned by using the resist pattern, then the device isolation recesses 1a are formed on the silicon substrate 1, and then the resist pattern is removed. Then, the SiO.sub.2 film of 15 nm thickness is formed on the inner surfaces of the device isolation recesses 1a by the thermal oxidation.

#### CLAIMS:

- 4. A semiconductor device according to claim 1, wherein the first semiconductor film and the second semiconductor film is formed of polysilicon respectively.
- 9. A semiconductor device manufacturing method according to claim 8, wherein the first semiconductor film and the second semiconductor film is formed of <u>polysilicon</u> respectively, and the polishing stop film is formed of a silicon nitride film.
- 17. A semiconductor device manufacturing method according to claim 16, wherein the gas consists of any one of a mixed gas of <u>silane</u> and hydrochloric acid, or a dichlorsilane gas, or a mixed gas of a dichlorsilane gas and hydrochloric acid.

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Search Results - Record(s) 1 through 2 of 2 returned.

1. Document ID: US 6649965 B2

L5: Entry 1 of 2

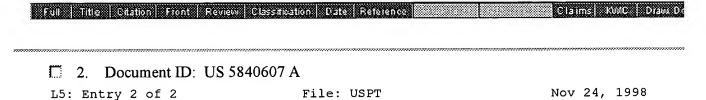
File: USPT

Nov 18, 2003

US-PAT-NO: 6649965

DOCUMENT-IDENTIFIER: US 6649965 B2

TITLE: Semiconductor device and method of manufacturing the same

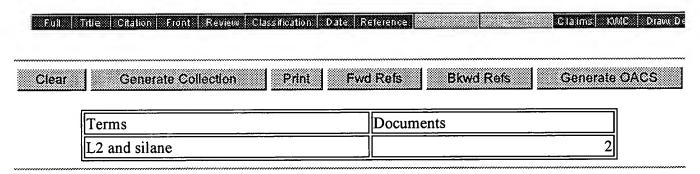


US-PAT-NO: 5840607

DOCUMENT-IDENTIFIER: US 5840607 A

TITLE: Method of forming undoped/in-situ doped/undoped polysilicon sandwich for

floating gate application



Display Format: TI Change Format

Previous Page

Next Page

Go to Doc#

## **Hit List**

Clear Generate Collection Print Fwd Refs Bkwd Refs
Generate OACS

### Search Results - Record(s) 1 through 10 of 11 returned.

1. Document ID: US 6709925 B1

L3: Entry 1 of 11

File: USPT

Mar 23, 2004

US-PAT-NO: 6709925

DOCUMENT-IDENTIFIER: US 6709925 B1

TITLE: Split-gate flash memory cell and manufacturing method thereof

Full Title | Citation | Front | Review | Classification | Date | Reference | Claims | NMC | Draw Do

US-PAT-NO: 6630392

DOCUMENT-IDENTIFIER: US 6630392 B2

TITLE: Method for fabricating flash memory device

Full Title Cration Front Review Classification Date Reterence Claims NMC Diam Do

3. Document ID: US 6624464 B2

L3: Entry 3 of 11 File: USPT Sep 23, 2003

US-PAT-NO: 6624464

DOCUMENT-IDENTIFIER: US 6624464 B2

TITLE: Highly integrated non-volatile memory cell array having a high program speed

Full Title Criation Front Review Classification Date Retainnee Claims KMC Draw D.

4. Document ID: US 6620684 B2

L3: Entry 4 of 11 File: USPT Sep 16, 2003

US-PAT-NO: 6620684

DOCUMENT-IDENTIFIER: US 6620684 B2

TITLE: Method of manufacturing nonvolatile memory cell

Full Title Citation Front Review Classification Date Reference Claims KMC Draws De 5. Document ID: US 6495467 B2

L3: Entry 5 of 11

File: USPT

Dec 17, 2002

US-PAT-NO: 6495467

DOCUMENT-IDENTIFIER: US 6495467 B2

TITLE: Method of fabricating a non-volatile memory device

Full Title Citation Front Review Classification Date Reference Claims AMC Draw.Dr

6. Document ID: US 6465293 B2

L3: Entry 6 of 11

File: USPT

Oct 15, 2002

Sep 24, 2002

US-PAT-NO: 6465293

DOCUMENT-IDENTIFIER: US 6465293 B2

TITLE: Method of manufacturing a flash memory cell

Full Title Offation Front Review Classification Date Reference Claims KWC Draw De 7. Document ID: US 6455374 B1

File: USPT

US-PAT-NO: 6455374

L3: Entry 7 of 11

DOCUMENT-IDENTIFIER: US 6455374 B1

TITLE: Method of manufacturing flash memory device

Full Title Citation Front Review Classification Date Reference Claims KWC Draw D 8. Document ID: US 6391716 B1

L3: Entry 8 of 11

File: USPT

May 21, 2002

US-PAT-NO: 6391716

DOCUMENT-IDENTIFIER: US 6391716 B1

TITLE: Method for forming poly spacer electron tunnel oxide flash with electric-

field enhancing corners for poly to poly erase

Full Title Citation Front Review Classification Date Reference Citatine NAME Draws Do

L2 and (hard adj mask)

9. Document ID: US 63	72564 B1	
L3: Entry 9 of 11	File: USPT	Apr 16, 2002
US-PAT-NO: 6372564 DOCUMENT-IDENTIFIER: US 63725	64 B1	
TITLE: Method of manufacturin	g V-shaped flash memory	
Full Title Citation Front Review	Classipostion Data Reference	Claims RMC Draw D
10. Document ID: US 6	362053 B1	
L3: Entry 10 of 11	File: USPT	Mar 26, 2002
US-PAT-NO: 6362053 DOCUMENT-IDENTIFIER: US 63620	53 B1	
TITLE: Flow process for produ of the sacrificial oxide	cing non-volatile memories wit	h differentiated removal
Full   Title   Citation   Front   Review	Glassification Date Reference	Claims FMC Draw D
Clear Generate Collection	Print Fwd Refs Bkwd	Refs Generate OACS
Terms	Docum	ients

Display Format: TI Change Format

Previous Page Next Page Go to Doc#

11

# **Hit List**

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Generat	3 COHECHON		Fwd Refs	Bkwd Refs
	Gener	rate OACS		

Search Results - Record(s) 11 through 11 of 11 returned.

11. Document ID: US 6339006 B1

L3: Entry 11 of 11

File: USPT

Jan 15, 2002

US-PAT-NO: 6339006

DOCUMENT-IDENTIFIER: US 6339006 B1

TITLE: Flash EEPROM cell and method of manufacturing the same

Full   Title   Citation   Front   Review   Classification   Date	Reference Claims KWC Draw. (
Clear Generate Collection Print F	wd Refs Bkwd Refs Generate OACS
Terms	Documents
L2 and (hard adj mask)	11

Display Format: TI Change Format

Previous Page

Next Page

Go to Doc#